## Remarks

The application was filed with claims 1-18. Claims 1-18 have been examined and are pending. Claims 1-18 are rejected. Claims 6 and 14 are amended. All rejections are traversed.

## **Interview Summary**

Date of Interview: 6 May 2003, (Telephonic), Takeguchi (Examiner) and Brinkman (35,4600 Attorney). The applicant notified the examiner that the office action contained an incorrect citation of Hodges in the body of the rejection. Since the applicant notified the office within one month of mail date of the action, the procedure set forth in MPEP 710.06 will be followed.

In paragraph 1, the Examiner notes the supplemental Office Action dated May 13, 2003 replaces the Office Action mailed 3/28/2003, after a telephone interview on May 6, 2003.

In paragraph 2, the Examiner requests cooperation in correcting errors. Claim 6 is amended to correct a clerical error.

In paragraph 3, the Examiner objects to informalities in claim 14. Claim 14 has been amended to overcome the objection.

In paragraphs 4-5, the Examiner rejected claims 1-18 under 35 U.S.C. 102(e) as being anticipated by Stallmo et al., (U.S. 6,289,398 - "Stallmo")

Independent claims 1, 8, and 15 are directed to a configurable RAID subsystem, comprising a user data array connected to a user application via a block I/O path *and* a configuration array connected to a configuration application *via the same block I/O path*.

Stallmo describes a distributed storage array system including a plurality of data storage devices (DSDs). Control of the plurality of DSDs is distributed among a plurality of Modular Control Units (MCUs), see, col. 4, lines 50-59. A first bus connects the MCU to a host 201, and a second bus connects the MCU to the associated DSD. A serial interface connects the MCUs in a bidirectional ring.

It is first noted, the first and second buses and serial ring described by Stallmo are **physical connections** that connect to **physical devices**, i.e., host, MCU, and DSD. It is well known in the art that physical buses always connect to physical devices, physical buses and serial interfaces **never** connect directly to applications (software). In fact, nowhere is there any teaching in the prior art that an application (software) can connect directly to physical buses (hardware).

Claimed is a (logical) block I/O path connected to a user application and a configuration application connected to the same block I/O path. The physical buses and serial interface of Stallmo can never anticipate the claimed path connected to the claimed application software.

In greater detail, the storage array of Stallmo, i.e., all nodes, may appear as a single device responding to a single identification number on the host bus, or as a number of independent devices. One of the MCUs is designated a controlling MCU. The controlling MCU receives either a read or write command and notifies the other MCUs that are involved in that read or write operation. Control of the host bus is transferred from one MCU to the next MCU in sequence to read or write data in the proper order, see Title, Abstract, Figures 203.

The invention uses the *same* block I/O **path** to connect the user data array to a user **application**, and the configuration array to a configuration **application**. A path connected to applications should not be confused with a physical bus connected to hardware.

In Stallmo, MCUs are connected to a host computer (physical hardware) via a host bus (physical hardware). DSDs (physical hardware) are connected to modular control units (physical hardware) via DSD buses (physical hardware). Each DSD bus is **independent** of the other and of the host bus, see, col. 6, line 59 – col. 7, line 6. If the buses are independent, they cannot be the **same** as claimed. MCUs further communicate configuration data over a serial bus connected in the bi-directional ring.

The Examiner points to col. 8, lines 31-33 as describing a "single block I/O path" connecting a user data array to a "user application," as well as connecting a configuration array to a "configuration application."

In the art, the meanings of application software, as claimed, and hardware devices as in Stallmo are very well distinguished, and never confused.

Applicants respectfully request the Examiner to respect this distinction.

The applicants reviewed the cited section to traverse the rejection in detail. The entire cited section states:

"When the invention is implemented using a SCSI host bus 207, input/output (I/O) requests are made using a command descriptor block."

The section is silent as to I/O block path. Further, the section only describes the physical SCSI host bus. Any I/O path to an **application**, as claimed, is never taught or suggested at all.

The Examiner is requested to state, with specificity, which words mean the *same* block I/O path to connect to a user application, *and* to a configuration application. The rejection by the Examiner is a mere conclusion, without a full development of reasons.

Further, the cited section is directed only to the host computer requesting read or write operation to one of the MCUs, which in turn access the data storage devices via a separate path, see above.

The section is completely silent as to application software. For these reasons alone, Stallmo can never anticipate what is claimed.

MPEP 2131 explicitly states that in order to anticipate a claim "each and every element as set forth in the claims" must be found in the prior art reference." The identical invention must be shown in as complete detail as is contained in the ... claim." Further, MPEP 707 states, "When a reference is complex or shows or describes inventions other than that claimed by the applicant, the particular part relied on must be designated as nearly as practicable. The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified." The Applicants request the Examiner point out, with specificity, which words, in the over 200 lines across 4 columns of Stallmo cited by the Examiner, mean 'user application' and 'configuration application' as claimed.

The applicants have thoroughly reviewed the reference, which only describes configuration tables stored on DSD connected to each MCU that are updated periodically by other MCUs, see, col. 10, lines 21-57. These are certainly not applications as claimed.

Regarding claim 2-3, 9, and 18, the Examiner's rejection states, in its entirety, "Also, Stallmo teaches the processing of configuration and user access commands via the block I/O path.

MPEP 706.07 makes clear that "the invention as disclosed and claimed should be thoroughly searched in the first action and the references should be fully applied." In the present application, the rejection fails not only to provide a reasonable rational as to how, in the Examiner's view, the applied art can be construed to teach each and every feature in the rejected claims,

but the rejection also fails to even consider explicitly claimed features of the invention as recited in claims 2-3, 9, and 18. In particular, wherein the user data array processes user data access commands executed by the user application, and the configuration application processes configuration commands, the user data access commands and the configuration commands communicated to the user data array and the configuration array respectively via the block I/O path.

Regarding claim 4, 10, 16 and 17 the Examiner is requested to state, with specificity, which words in col. 8, line 40 to col. 11, line 57, mean "configuration array," "user data array includes a dynamic identification assigned by the configuration array," "static configuration identification" or "the configuration array includes a static configuration identification." The rejection by the Examiner is a mere conclusion, without a full development of reasons.

In claims 5 and 11 a configuration write command is assembled an executed in the configuration application, the configuration write command is processed in the configuration array and a status on the processing of the configuration write command is returned to the configuration application via the block I/O path. As stated above, Stallmo never taught or suggested any I/O path to an **application**, as claimed. Therefore, Stallmo can never anticipate what is claimed.

In claims 6 and 7, the configuration application reads a predetermined block of the configuration array to obtain an associated application identification using the same (logical) block I/O path as used by the user data application and array. Stallmo only describes physical hardware, i.e., host bus and DSD bus at col. 11, lines 29-37. Stallmo never describes block I/O paths between applications and arrays as claimed. The physical connections between hardware devices can never anticipate what is claimed.

Further, in claims 7 and 13, a configuration write command is assembled and executed in the configuration application, the configuration write command including a request to read a configuration information data structure and the application identification. The configuration write command is processed in the configuration array; a configuration read command is assembled and executed in the configuration application, the configuration read command including the application identification; the configuration read command is processed in the configuration array; and the requested configuration information data structure and status is returned to the configuration application. All of the above steps occurring between the configuration application and the configuration array use the same block I/O path connecting the user data array to the user application. The physical connections described in Stallmo can never anticipate what is claimed.

Regarding claim 14, Stallmo send his lock request over the serial connection between MCUs, which cannot be the same block I/O path as connects the user data array to the user application as claimed.

All rejections have been complied with, and applicant respectfully submits that the application is now in condition for allowance. The applicant urges

the Examiner to contact the applicant's attorney at phone and address indicated below if assistance is required to move the present application to allowance.

Respectfully submitted,

Andrew J. Curtin Reg. No. 48,485

Correspondence:

Mr. Chris Franklin RAIDCore, Inc. Suite 304 71 Spit Brook Road Nashua, NH 03060